REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The Office Action dated June 29, 2005, has been received and its contents carefully reviewed.

Claims 1-21 remain pending in this application. Applicant wishes to thank the Examiner for the indication that claims 3-6, 11-15, and 19 contain patentable subject matter.

In the Office Action, claims 1, 2, 7-10, 16-18, 20 and 21 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,078,317 to Sawada (hereinafter "Sawada").

The rejection of claims 1, 2, and 7 is respectfully traversed and reconsideration is requested. Claims 1, 2, and 7 are allowable over the cited references in that each of these claims recites a combination of elements including, for example, "setting reference modulated data," "detecting a driving frequency of video image data for a current frame," and "adjusting the reference modulated data in accordance with the detected driving frequency to modulate the video image data." Sawada does not teach or suggest at least these features of the claimed invention.

Sawada is directed to a invention for displaying different video formats (*e.g.*, VGA, SVGA, *etc.*) on a liquid crystal display (LCD) having a fixed number of pixels. Sawada provides an example of an LCD having display size of 1,280x960 pixels. (Col. 4, ll. 54-58.) VGA display signals include data for 640x480 pixels. Therefore, the VGA display signal has one fourth the number of pixels available on the LCD display. Therefore, the VGA signal must be processed in order to fill the whole screen. In the horizontal direction, the signal is an analog signal with the desired value for each of the 640 horizontal display pixels as it would scan across the display in a traditional cathode ray tube type of display. In order to provide data to 1280 pixels in the horizontal row, the horizontal VGA signal is sampled 1280 times by the ADC 13. (Col. 3, ll. 61-65; col. 5, ll. 33-36.) For the VGA signal, the number of vertical lines of the display (960) is twice the number of vertical lines in the VGA signal (480). Therefore, each of the vertical lines in the VGA signal is displayed on two horizontal lines of the display by a control signal supplied to the scanning control circuit 22. (Col. 5, ll. 43-45.) In the case of an SVGA signal with for example 1,024x768 pixels, the horizontal VGA signal is again sampled to produce 1,280 samples for the 1,280 horizontal pixels. In the vertical direction though, the

number of lines in the display is 1.25 times the number of vertical lines in the SVGA signal. Therefore, a simple line doubling cannot be done. In order to display the 768 lines in the SVGA signal on the display with 960 vertical lines, the data is interpolated by the interpolating processing circuit 16. (Col. 5, ll. 51-60; col. 4, ll. 1-9.)

The display control apparatus of Sawada has a display mode discriminator 15 that discriminates the current display mode on the basis of the timings, polarities, and the like of the synchronizing signals. (Col. 3, ll. 49-60.) Further Sawada states: "The display mode detector 15 supplies the detection result to a display mode dependence controller 17." (Col. 3, ll. 53-55.) The display mode dependence controller 17 then controls the display control apparatus as shown in the flow chart of Fig. 5. (Col. 6, ll. 17-18.) The controller 17 receives display mode information detected by the display mode detector 15 in step S1. This information is used in step S2 to determine which display mode is used in the input display signal. Depending in the display mode, the process continues to either step S3, S5, or S7, where the low pass filter and VCXO are selected in the clock generator 14 to generate the correct dot clocking signal for use in the display control apparatus corresponding to the display mode. Next, the interpolation steps S4, S6, or S8 are performed according to the display mode.

The examiner identifies the ADC 13 and interpolation processing circuit 16 as "setting reference modulated data." As discussed above the ADC samples the horizontal line signal to produce the number of data samples corresponding to the horizontal resolution of the display. Then the interpolating processing circuit 16 stores horizontal lines of data to use to interpolate between the lines to produce the number of vertical lines of data corresponding to the vertical resolution of the display, *e.g.*, converting 768 vertical lines into 960 vertical lines. The output of the interpolating processing circuit 16 are interpolated display data. In the present invention, reference modulated data represents a voltage level necessary to drive a pixel cell to a desired state based upon the previous voltage level in the pixel. Because of the relatively slow response times of some types of liquid crystal compared to the scan time of the display, the pixels need to be driven with a lower or higher voltage than would normally be required to achieve the desired state of the LCD to produce the desired brightness in the allotted scan time. The values produced by the ADC 13 and the interpolation processing circuit 16 are completely different, so they are not reference modulated data as claimed.

Further, the Examiner states that the display control apparatus of Sawanda detects "a driving frequency of video image data for a current frame" using the clock generator 14, the display mode detector 15, and the display mode dependence controller 17." Further, the Examiner states: "Sawada clearly discloses LPFs 33 to 35 are low-pass filter having high-input impedance, each of which filters a frequency signals in corresponding to each of the horizontal frequencies of the respective display such that three different horizontal frequencies (e.g. 31.5 KHz, 37.8 KHz and 48.3 KHz) inputted from 31 can be detected. . ." The LPFs 33 to 35 are in the clock generator that actually generates a dot clock signal based upon control inputs from the display mode detector 15 and the display mode dependence controller 17. The LPFs 33 to 35 are not used to detect the driving frequency of video image data as asserted by the Examiner. The display mode detector 15 as discussed above determines the display mode of the input video signal from a number of characteristics of that signal. The driving frequency of the signal is then known or infered because specific drive frequencies are associated with each display mode of the video signal. Sawada actually infers the drive frequency of the video image data from other information, rather than detecting it as called for in the claimed invention.

Finally, the examiner identifies the interpolation processing circuit 16, the γ characteristic adjustment circuit 19, and the halftone processing circuit 21 as adjusting the reference modulated data in accordance with the detected driving frequency to modulate the video image data. As stated above, Applicant asserts that Sawada does not teach reference modulated data and detecting the driving frequency of the video image data, so this feature is cannot be taught by Sawada. But even if Sawada did teach these elements, it does not adjust "the reference modulated data in accordance with the detected driving frequency to modulate the video image data." The processing performed by the interpolation processing circuit 16, the γ characteristic adjustment circuit 19, and the halftone processing circuit 21 depend on the display mode, *i.e.*, VGA, SVGA, of the input video image data not the driving frequency thereof. This processing as discussed above is intended to process display signals that have fewer pixels than in the display. Thus, the data in the display signal needs to be expanded to fit on the actual display. The actual drive frequency is not used to actually change the value of the display data, but rather the number of pixels associated with the display mode is used.

Accordingly, for the various reasons stated above, claims 1, 2, and 7 are allowable over Sawada.

The rejection of claims 8 and 9 is respectfully traversed and reconsideration is requested. Claims 8 and 9 are allowable over the cited references in that each of these claims recites a combination of elements including, for example, "setting reference modulated data," "setting a different weighting value for each frequency band," and "assigning a weighting value of the frequency band including the driving frequency to the reference modulated data to adjust the reference modulated data, thereby modulating the video image data." Sawada does not teach or suggest at least these features of the claimed invention. The discussion above regarding claim 1 applies to these claims as well. Accordingly, claims 8 and 9 are allowable over Sawada.

The rejection of claims 10, 16-18, 20, and 21 is respectfully traversed and reconsideration is requested. Claims 10 and 16 are allowable over the cited references in that each of these claims recites a combination of elements including, for example, "a mode detector detecting a driving frequency of current video image data" and "a modulator selecting reference modulated data from previously registered data and adjusting the selected reference modulated data in accordance with the detected driving frequency." Claims 17, 18, 20, and 21 are allowable over the cited references in that each of these claims recites a combination of elements including, for example, "a mode detector detecting a driving frequency of current video image data" and "a modulator selecting reference modulated data from previously registered data, setting a different weighting value for each frequency band having a plurality of frequency ranges, and assigning a weighting value of the frequency band including the detected frequency to the reference modulated data." Sawada does not teach or suggest at least these features of the claimed invention. The discussion above regarding claim 1 applies to these claims as well. Accordingly, claims 10, 16-28, 20, and 21 are allowable over Sawada.

Applicants believe the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. § 1.136, and any additional fees required under 37

C.F.R. § 1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. *A duplicate copy of this sheet is enclosed.*

The undersigned hereby signs this filing under the authority provided by 37 C.F.R. § 1.34 pending the filing of a Power of Attorney and Statement under 3.37(b) executed by Assignee.

Respectfully submitted,

Dated: September 29, 2005

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